Your Gateway to Global Success

SEMESTER LEARNING PLAN
(RENCANA PEMBELAJARAN SEMESTER)
No. Doc: SLP/ BE /D721-1FTLB

Course Name	**: Biology Lab**
Course Code	**: D721-1FTLB**
Credit	**: 3 SKS/ 4 ECTS**
Semester	**: 3**
Course Status	**: Mandatory**
Prerequisite/s	**: Electrical Engineering 2**
Faculty	**: Life Sciences & Technology**
Study Program	**: Biomedical Engineering**
Concentration	**: -**
Degree	**: Bachelor**
Instructor(s)	**: Aulia Arif Iskandar**
Delivery Mode	**: Hybrid**
Learning Method	**: Blended Learning**
Total Activity Time[1]	**: 135 hours**
Scheduled Session[2]	**: 35 hours**
Independent Study	**: 98 hours**

[1] 1 credit equals to 45 hours of learning activities (including guided, structured assignment, & independent study) per semester
[2] total sessions x total SKS x 50 minutes

Course Description	This course is an introduction to digital electronics that will cover the basic concepts, tools, and techniques in designing and analyzing digital systems. The course begins by explaining the fundamentals of digital electronics, including analog versus digital logic, number systems, and logic gates. We will then progress through various topics in digital electronics, including Boolean algebra, Karnaugh maps, flip-flops, counters, and timers. The course will also cover the use of digital electronics software simulation tools, such as TinkerCAD, for circuit design and testing. Additionally, students will learn how to use Eagle and FreeCAD software for printed circuit board (PCB) design and 3D modeling.
Learning Outcomes	***Graduate Learning Outcomes (CPL) assigned to this course**
	CPL 1 (P1): Understand the theoretical concepts of natural science, human anatomy & physiology, biochemistry, biophysics, engineering mathematics applications, engineering principles, engineering science and engineering design required for the analysis and design of systems, products or components related to biomedical engineering applications. CPL 2 (P3): Understand the principles and techniques of designing systems, processes, or components related to Biomedical Engineering;. CPL 3 (KU1): Apply logical, critical, systematic, and innovative thinking in the context of developing or implementing health science and technology.
	***Course Learning Outcomes (CPMK)**
	CPMK 1: Understand the basics of digital electronics and the differences between analog and digital systems. CPMK 2: Design and simulate logic circuits using Boolean algebra and Karnaugh maps. CPMK 3: Understand and analyze various types of flip-flops and counters, including asynchronous and synchronous designs. CPMK 4: Design and simulate basic arithmetic circuits, including adders and subtractors. CPMK 5: Use software tools, including TinkerCAD, Eagle, and FreeCAD, for circuit design, testing, and PCB design.
	***Planned Final Ability (Sub-CPMK, if any)**
	Sub-CPMK X: ..... Sub-CPMK X: ..... Sub-CPMK X: .....

References	**Primary Reference:** Digital Electronics: Principles and Applications, 10th Ed., by Roger L. Tokheim ISBN: 978-0073373874
	Additional Reference:

Session	Topic/ Subtopics	Learning Outcomes	Assessment Criteria		Student Learning Experiences/Activities	Learning Methods and Modalities	Allocation Time		Learning Materials
			Indicator	Weight (%)			Scheduled (@50 Min)	Independent Study (@Hours)	
1	Introduction to Digital Electronics	CPMK 1, CPMK 5 (2 outcomes)	Hands-on TinkerCAD using basic parts	5%	• Lecture materials: Course Syllabus, Chapter 1 and 2.	Synchronous	3	7	**GCR Material:** PDF/GSlides Introduction to Digital Electronics and Syllabus, Chapter 1 and Chapter 2 **GCR Quiz/Assignment:** Practice TinkerCAD using basic parts
2	Digital Numbers and Logic Gates, NAND-Gate	CPMK 1, CPMK 2, CPMK 5 (3 outcomes)	TinkerCAD simulation of basic logic gates (AND, OR, NOT, NAND)	7%	• Lecture: Number systems, basic logic gates, NAND as universal gate. • TinkerCAD lab: Implementing and testing logic gates.	Synchronous			
3	Combinational Logic, Combinational Logic Gates SOP & POS	CPMK 2, CPMK 5 (2 outcomes)	Design and simulate combinational circuits (SOP/POS) in TinkerCAD	5%	• Lecture: Intro to combinational logic, Sum of Products, Product of Sums. • TinkerCAD lab: Building combinational circuits from Boolean expressions.	Synchronous			
4	Boolean Expression, K-Map, Logic Gate Combination and Simulation, Simulation	CPMK 2, CPMK 5 (2 outcomes)	Simplify Boolean expressions using K-Maps and simulate in TinkerCAD	5%	• Lecture: Boolean algebra, Karnaugh maps for simplification. • TinkerCAD lab: Designing optimized circuits from K-Maps.	Synchronous			

	Combinational Logic Gates								
5	IC Specification and Interfacing using Relays, Basic of Flip-Flops	CPMK 1, CPMK 3, CPMK 5 (3 outcomes)	Understanding IC datasheets and basic flip-flop simulation in TinkerCAD	7%	• Lecture: Reading IC datasheets, relay interfacing, introduction to sequential logic & flip-flops (SR, D). • TinkerCAD lab: Simulating basic flip-flop behavior.	Synchronous			
6	Flip-Flops, Ripple Counter	CPMK 3, CPMK 5 (2 outcomes)	Design and simulate asynchronous ripple counters in TinkerCAD	5%	• Lecture: JK, T flip-flops, asynchronous counter design. • TinkerCAD lab: Building and testing ripple counters.	Synchronous			
7	Up- and Down-Counter using JK-Flip-Flop, Up-Counter with Seven Segment	CPMK 3, CPMK 5 (2 outcomes)	Design and simulate synchronous Up/Down counters with 7-segment display interface in TinkerCAD	5%	• Lecture: Synchronous counter design (Up/Down), interfacing with 7-segment displays. • TinkerCAD lab: Building JK-FF based Up/Down counter and displaying output.	Synchronous			
8	Up-counter using 74LS73 and LEDs on NI ELVIS, Up-counter JK-FF plus Reset Circuit	CPMK 3, CPMK 5 (2 outcomes)	Implement JK-FF counter with specific IC (e.g., 74LS73 simulated) and reset functionality in TinkerCAD	5%	• Lecture: Practical IC usage (74LS73), counter reset mechanisms. • TinkerCAD lab: Simulating 74LS73 based counter, adding reset. (NI ELVIS part would be physical lab)	Synchronous			
9	Pulse wave using 555, Quartz Crystal 32.768 kHz	CPMK 1, CPMK 3, CPMK 5 (3 outcomes)	Simulate 555 timer astable multivibrator in TinkerCAD and understand crystal oscillators	7%	• Lecture: 555 timer IC (astable mode), crystal oscillators for clock generation. • TinkerCAD lab: Designing a 555 astable circuit.	Synchronous			
10	555 Astable Simulation and 32.768 kHz	CPMK 3, CPMK 5 (2 outcomes)	Design and simulate a 1Hz clock generator	4%	• Lecture: Frequency division using ICs (CD4060), combining components for a 1Hz signal.	Synchronous			

	crystal, 1 Hz Generator using 32.768 kHz, CD4060, 74LS73		circuit in TinkerCAD		• TinkerCAD lab: Simulating a 1Hz generator.				
11	Digital Clock Final Project I, Up-Counter Schematics Design	CPMK 2, CPMK 3, CPMK 4, CPMK 5 (4 outcomes)	Initial schematic design for digital clock modules (seconds/minutes) in TinkerCAD	9%	• Lecture: Digital clock project overview, modular design (seconds, minutes). • TinkerCAD lab: Start schematic for up-counters (0-59).	Synchronous			
12	NAND Gate for Up-Counter Reset, Final Project Digital Clock Schematics Design	CPMK 2, CPMK 3, CPMK 4, CPMK 5 (4 outcomes)	Design counter reset logic (e.g., reset at 60) using NAND gates and complete module schematics in TinkerCAD	9%	• Lecture: Counter reset logic design, integrating modules. • TinkerCAD lab: Implementing reset logic for counters (0-59), hour counter (0-11 or 0-23).	Synchronous			
13	Final Project: Digital Clock using D-FF and XTAL 32.768kHz, Digital Clock Hour reset, up-counter 1 to 12	CPMK 2, CPMK 3, CPMK 4, CPMK 5 (4 outcomes)	Design and simulate hour counter with reset (1-12 or 0-23) and integrate clock modules in TinkerCAD	9%	• Lecture: Hour counter design (1-12 or custom range), overall clock integration. • TinkerCAD lab: Designing hour module, integrating all clock parts (seconds, minutes, hours).	Synchronous			
14	Final Project: Digital Clock using D-FF and XTAL 32.768kHz (Continued)	CPMK 2, CPMK 3, CPMK 4, CPMK 5 (4 outcomes)	Testing and debugging of the complete digital clock simulation in TinkerCAD	9%	• Lab: Finalizing digital clock project, testing, debugging. • Peer review/Instructor feedback.	Synchronous			
15	Final Project: Digital Clock using D-FF and XTAL 32.768kHz (Conclusion/Presentation)	CPMK 2, CPMK 3, CPMK 4, CPMK 5 (4 outcomes)	Submission and optional presentation/demonstration of the final digital clock project	9%	• Lab: Final project submission. • Optional: Project demonstration/ Q&A.	Synchronous			

Notes:
[Please Add Notes]

Prepared by:	Reviewed by:	Approved by:
Head of Editorial Team	Head of Dept……	Dean of……..